

DERWENT-ACC-NO: 2003-694288

DERWENT-WEEK: 200366

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TITLE: Insulating tape for semiconductor chip package
using
copper lead frame

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PATENT-FAMILY:

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ABSTRACTED-PUB-NO: KR2002078839A

BASIC-ABSTRACT:

NOVELTY - An insulating tape for a semiconductor chip package of a lead-on-chip (LOC) type, especially using a copper lead frame, is provided to improve reliability of the package by adjusting a coefficient of thermal expansion (CTE) of the insulating tape on the level of the copper lead frame.

DETAILED DESCRIPTION - The insulating tape has a three-layered structure in which an adhesive layer(6) is formed on both sides of a base film(5). In particular, the entire insulating tape has a CTE ranging from 16.0 to 23.5 ppm/

deg. C. The base film(5) is formed of heat-resistant resin such as polyimide, polyphenylene sulfide, polyether, polyparabanic, polyethylene terephthalate, or fluororesin. The adhesive layer(6) is formed of thermosetting or thermoplastic adhesive such as polyimide or polyamideimide. The adhesive layer(6) has a CTE of 20-300 ppm/ deg. C. The copper lead frame includes copper of 98.5% and over.

CHOSEN-DRAWING: Dwg.1/10

TITLE-TERMS: INSULATE TAPE SEMICONDUCTOR CHIP PACKAGE COPPER LEAD FRAME

DERWENT-CLASS: A85 L03 U11

CPI-CODES: A12-E07C; L04-C12E; L04-C17D;

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